UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,454	12/20/2000	Richard Dennis Beckert	MS1-727US	2558

22801 7590 05/11/2004

LEE & HAYES PLLC
421 W RIVERSIDE AVENUE SUITE 500
SPOKANE, WA 99201

EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 05/11/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,454	BECKERT ET AL.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 32-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 32-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings (figures 1 and 12A-12B) were received on 06 April 2004. These drawings are approved by the Examiner.

Specification

2. Applicant's amendments to the abstract and specification are acknowledged. However the amendments are not in the proper format in accordance with 37 CFR 1.121 and cannot be entered. In particular, the amendments to the abstract and specification do not show the changes relative to the immediate prior version of the abstract and specification paragraphs. See 1267 OG 106 (25 February 2003).

The abstract and specification amendments in the proper format are required in response to this action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Saadeh et al (5,283,905).

As per claim 32, Saadeh et al. teaches, as shown in figure 7, a computing device including a SRAM 70, battery 100, analog power control 614 for detecting when the +12 volt or +5 volt sources fall outside the threshold voltages (i.e. "dropped out of regulation"), and battery load regulation 600, which turns on the battery based on an initiate battery signal 622 from the analog power control. See also column 16, lines 28-36. The analog power control 614 and the battery load regulation collectively represent "power control circuitry". The battery is thereafter connected to the SRAM.

Note that the above 35 U.S.C. 102(b) rejection for claim 32 is given based on the fact that "automotive", although in the preamble, is not in the body of the claim and does not add any patentable weight to the claims in question.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 8, 10, 15-16, 32, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Mills et al. (5,696,917).

Applicant's admitted prior art ("APA") teaches that it was known to provide computing devices in automobiles (see page 1, lines 6-7). The computing devices in automobiles, as generally shown in figure 1, include a non-volatile storage 12 (generally FLASH memory; see page 2, lines 21-23) and a DRAM 14. Upon boot-up, the object store of the computing device is

copied from the non-volatile storage 12 to the DRAM 14 (see page 3, lines 1-2). When the automobile computing device enters a zero power mode, the contents of the DRAM are written back to the non-volatile memory 12. The computing device would include a computer (i.e. processor).

As per claims 1, 8, and 32, the "APA" does not teach a static random access memory (SRAM) connected to a battery for preserving one or more pages in the event of power loss. Mills et al. teaches, with reference to figure 2, a computing system including a FLASH memory 230 and a battery backed SRAM 240. The SRAM 240 functions as a write cache for the FLASH memory ("operatively associated with the non-volatile memory"). See also column 11, lines 34-40. It would have been obvious to one of ordinary skill in the art to have added a SRAM write cache to the automotive computing system set forth by the "APA", as suggested by Mills et al., because Mills et al. teaches that such an addition would enhance execution speed (see column 12, lines 17-19), while the SRAM would be faster to write to or read from than DRAM (see column 12, lines 10-16). Furthermore, connecting the SRAM to a battery would prevent read/write files from being lost as set forth at column 10, lines 51-53.

As per claim 2, "APA" teaches at page 2, lines 21-23, that the non-volatile memory is a FLASH memory.

As per claim 3, "APA" teaches at least one DRAM 14.

As per claim 4, Mills et al. teaches coupling a battery back-up to a SRAM in the event of a power failure of the primary power source. See column 3, lines 58-60. Therefore, the combination of "APA" and Mills et al. teaches coupling a battery back-up to the SRAM in the event of a power failure of the primary power source, namely the automobile power source.

As per claims 10 and 24, the claim is rejected for the reasons set forth for claims 1 and 4-5, above.

As per claim 15, "APA" teaches a non-volatile memory coupled to the processor and contains the object store for the automotive computing system. See the discussion for claim 1, above.

As per claim 16, "APA" teaches that the non-volatile memory is a FLASH memory (see page 2, lines 21-23, of the specification).

As per claim 17, while the combination of "APA" and Mills et al. teaches a system including a non-volatile FLASH memory, DRAM, and SRAM, the combination does not explicitly teach that the SRAM is configured to receive object store pages from the DRAM (claims 17-18), which stores only read only pages (claim 18), which have been written to (claims 19-20). It would have been obvious to one of ordinary skill in the art to have the SRAM receive read only pages from the DRAM that have been written, because Mills et al. suggests that a SRAM write cache would provides faster access to data than the DRAM (see column 12, lines 10-16) and would provide data security for pages that have been written (i.e. dirty) should the system power be lost (see column 10, lines 51-53). It would have been further obvious to keep the DRAM for use in storing read-only pages (such as application programs which are primarily read-only pages and take up a large portion of memory) because Mills et al. teaches that DRAM can hold four times as much data as an SRAM of the same complexity (see column 3, lines 34-38).

As per claim 36, the claim is rejected for the reasons set forth for claims 1 and 4, above.

7. Claims 6-7 and 33, are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA" and Mills et al., and further in view of Heyden et al. (5,798,961).

The combination of "APA" and Mills et al. does not teach that battery back-up for the SRAM is a single cell battery or a lithium battery. Heyden et al. teaches the use of a single cell lithium battery in backing up a SRAM. See column 3, lines 60-67. It would have been obvious to have utilized a single lithium cell battery for the battery back-up in the combination of "APA" and Mills et al. because Heyden et al. teaches that a single lithium battery cell has a high energy density, high cell voltage, wide thermal operating range, and low self discharge (see column 3, line 66, to column 4, line 4).

8. Claims 5, 9, 11-12, 21-23, 25-26, 28, 34-35, 37, 39-40, 43-44, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA" and Mills et al., and further in view of Saadeh et al. (5,283,905).

As per claims 9, 25, 31, and 34-35 the combination of "APA" and Mills et al. teaches the invention as set forth for claims 1 and 8, above. However, the combination of "APA" and Mills et al. does not particularly teach "circuit means for detecting a power loss and responsive thereto operably coupling the battery with the SRAM in the event of an automotive power loss". Saadeh et al. teaches as shown in figure 7, a computing device including a SRAM 70, battery 100, analog power control 614 for detecting when the +12 volt or +5 volt sources fall outside the threshold voltages and battery load regulation 600, which turns on the battery based on an initiate battery signal 622 from the analog power control. See also column 16, lines 28-36. The analog power control 614 and the battery load regulation collectively represent "circuitry means". It would have been obvious to one of ordinary skill in the art to have modified the combination of

"APA" and Mills et al. to include circuitry to monitor and control the flow of supply power, as taught by Saadeh et al., because this would provide efficient protection of the volatile data in the system (see column 2, lines 16-24) as well as providing for battery power conservation (see column 1, lines 28-29).

As per claims 5 and 11, these claims are rejected for the reasons set forth for claim 9, above, noting that the "means for operably coupling" of claim 5 and the "power control circuitry" of claim 11 corresponds to the "circuit means" of claim 9.

As per claims 21-23 and 39, the claims are rejected for the reasons set forth for claims 10-11 and 36. However, the combination of "APA", Mills et al., and Saadeh et al. does not teach that the "low voltage detection circuitry" (equivalent to the "power control circuitry" of claim 11) generates a signal to the processor to indicate that the voltage has dropped out of regulation and that a copy operation from the DRAM to the SRAM should be initiated. However, it would have been obvious to one of ordinary skill in the art to have modified the combination of "APA", Mills et al., and Saadeh et al. such that the when the voltage drops out of regulation the processor is signaled and initiates a copy operation from the DRAM to the SRAM because this would save modified data to a fast non-volatile memory prior to losing power (which is suggested by "APA" at page 3 when discussing copying data from DRAM to FLASH memory).

As per claim 26, Saadeh et al. teaches that the battery 100 consists of 5 rechargeable battery cells. See column 16, lines 8-9.

As per claims 12, 28, and 37, Saadeh et al. teaches that the analog power control 614 entering a power mode other than a normal power mode when the +12 or +5 volt are above or below threshold settings. See column 16, lines 24-27. The next appropriate power mode is

entered with is either a reserve or standby mode, both representing a "low power state". See column 16, lines 54-67.

As per claim 40, the claim is rejected for the reasons set forth for claims 10 and 12, above.

As per claim 43, this claim is rejected for the reasons set forth for claims 1 above, further noting that it would have been obvious to one of ordinary skill in the art to have modified the combination of "APA", Mills et al., and Saadeh et al. such that the when the voltage drops out of regulation a copy operation from the DRAM to the SRAM is initiated because this would save modified data to a fast non-volatile memory prior to losing power (which is suggested by "APA" at page 3 when discussing copying data from DRAM to FLASH memory). Furthermore, it would have been obvious to one of ordinary skill in the art to have the SRAM receive pages from the DRAM that have been written, because Mills et al. suggests that a SRAM write cache would provides faster access to data than the DRAM (see column 12, lines 10-16) and would provide data security for pages that have been written (i.e. dirty) should the system power be lost (see column 10, lines 51-53).

As per claim 44, Saadeh et al. teaches that the analog power control 614 entering a power mode other than a normal power mode when the +12 or +5 volt are above or below threshold settings. See column 16, lines 24-27. The next appropriate power mode is entered with is either a reserve or standby mode, both representing a "low power state". See column 16, lines 54-67.

As per claim 48, this claim is rejected for the reasons set forth in claims 43-44, above.

9. Claims 14, 30, 41, 45, 47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA", Mills et al., and Saadeh et al., in further view of Clohset (5,384,747).

As per claims 14, 30, 41, 45, 47, and 49, the claims are rejected for the reasons set forth for claims 11, 25, 40, and 43 (respectively), above. However, the combination of "APA", Mills et al., and Saadeh et al. does not teach placing the SRAM in a low power state prior to coupling the SRAM to the battery back-up. Clohset teaches placing the SRAM in the low power state prior to coupling the SRAM to the battery. See column 2, lines 40-43. It would have been obvious to one of ordinary skill in the art to have place the SRAM in a low power state prior to coupling the SRAM to the battery, as taught by Clohset, because Clohset teaches that this would prevent data loss in the SRAM. See column 2, lines 40-44. Clohset teaches placing the SRAM in a low power state to avoid loss of data stored in the SRAM and avoid draining the battery. See column 2, lines 36-38.

10. Claims 13, 29, 42, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA", Mills et al., and Saadeh et al., in further view of Price (5,604,709).

As per claims 13, 29, 42, and 46, the combination of "APA", Mills et al., and Saadeh et al. does not teach isolating the SRAM and the battery back-up. Price teaches that it was known to isolate the SRAM from other circuits on the computer when entering a low power state. See column 2, lines 52-57. It would have been obvious to one of ordinary skill in the art to have isolated the SRAM (and battery) from other system components, as taught by Price, because Price teaches that isolating the SRAM would prevent leakage current that could drain the battery

(see column 2, lines 57-58), thereby ensuring that the battery's capacity does not diminish quickly (see column 2, line 55).

11. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA", Mills et al., and Saadeh et al. and further in view of Heyden et al. (5,798,961).

As per claim 27, the combination of "APA", Mills et al., and Saadeh et al. does not teach that battery back-up for the SRAM is a single cell battery or a lithium battery. Heyden et al. teaches the use of a single cell lithium battery in backing up a SRAM. See column 3, lines 60-67. It would have been obvious to have utilized a single lithium cell battery for the battery back-up in the combination of "APA", Mills et al., and Saadeh et al. because Heyden et al. teaches that a single lithium battery cell has a high energy density, high cell voltage, wide thermal operating range, and low self discharge (see column 3, line 66, to column 4, line 4).

12. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of "APA", and Mills et al. in further view of Clohset (5,384,747).

As per claim 38, the claim is rejected for the reasons set forth for claim 36, above, noting that Clohset teaches placing the SRAM in the low power state prior to coupling the SRAM to the battery. See column 2, lines 40-43. It would have been obvious to one of ordinary skill in the art to have place the SRAM in a low power state prior to coupling the SRAM to the battery, as taught by Clohset, because Clohset teaches that this would prevent data loss in the SRAM. See column 2, lines 40-44. Clohset teaches placing the SRAM in a low power state to avoid loss of data stored in the SRAM and avoid draining the battery. See column 2, lines 36-38.

Response to Arguments

13. Applicant's arguments filed 06 April 2004 have been fully considered but they are not persuasive.

With respect to the rejection of claim 32 under 35 U.S.C. §102(b), Applicant states that the rejection of claim 32 is moot since the claim depends from claim 25, which has been amended. However, claim 32 is an independent claim and has not been amended. The rejection is maintained.

With respect to the rejection of the claims under 35 U.S.C. §103(a), Applicant states that "Mills teaches away from the embodiment in the APA by advocating against the inclusion of a volatile DRAM in the asynchronous non-volatile memory" (pages 17-18 of the response). However, Mills et al. is not relied upon to teach adding a DRAM to APA; instead Mills et al. is relied upon to teach adding a SRAM to the system of APA for the reasons stated in the rejection. Mills et al. does not teach away from adding an SRAM to a system including a FLASH main memory, nor does it teach away from APA by teaching removing a DRAM from a system with FLASH main memory.

Furthermore, figures 13 and 15 have not been relied upon by the Examiner. The fact that they do not show an SRAM in the computer system is not relevant, since other portions of Mills et al. teaches utilizing an SRAM in a system with a FLASH main memory.

Finally, Mills et al. teaches the desirability of adding SRAM to a system as set forth at column 12, lines 10-16 and 17-19.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(703) 746-5693**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
May 5, 2004